REMARKS

As stated on page 2 of the Office Action, the Examiner has rejected claims 1,3-9, 11- 12, 14-21 and 23-28 under 35 USC 103(a) as being unpatentable over Bates at al, U.S. Patent 7,080,360, Rodgers et al , U.S. Patent 5,517,657, in view of Pardo et al, U.S. Patent 5,754,839.

As stated on page 9 of the Office Action, claim 10 is rejected under 35 USC 103(a) as being unpatentable over Bates at al, U.S. Patent 7,080,360, Rodgers et al, U.S. Patent 5,517,657, in view of Pardo et al, U.S. Patent 5,754,839, further in view of Master et al, U.S.patent 6,836,839.

Bates describes a method, apparatus and article of manufacture for debugging code (Abstract). Bates is not oriented towards stream computers with functional units interconnected by programmable switches for reconfiguring said stream computer. Bates does not envision multiple data flows within a stream computer, and their interaction to arrive at a viewpoint descriptive of the data based on a debug stream. In contrast to the present application, Bates uses conventional Von Newman computer architecture of the prior art, described in Fig 1 of the present application. Bates does not suggest applying its teachings to a reconfigurable computer having multiple functional units operating concurrently and independently in response to tokens as in the stream computer described herein. Bates does not teach nor suggest, nor would the teachings in Bates be applicable, in a multiple stream environment where a data stream and a debug stream are being received by independently operating functional units.

Because of the structural differences between Bates and the present application, Bates does not envision multiple data and other flows within a computer having multiple functional units responsive to tokens, and their interaction to arrive at a viewpoint descriptive of the data based on a debug stream. The teachings in Bates are not applicable in a multiple functional units environment where a data stream containing tokens and a debug stream are present. Bates does not have, suggest, nor describe any switching means or other means for re-configuring multiple, concurrently

operating, independent functional units.

Further distinguishing from Bates, the present claims have been amended to include structural details referencing said interconnected functional units computing independently and programmable switches programmably reconfiguring said plurality of interconnected functional units to direct said data stream among said interconnected functional units in accordance with programming commands.

The effect of tokens on the data contained in the data stream is now further distinguished from Bates. The tokens identify how independent, concurrently operating functional units are to operate on the data stream. Bates does not have tokens in its data stream, nor can change how the data is to be operated on in accordance with these tokens.

Rodgers at al, U.S. Patent 5,517,657, filed March 30, 1994 is titled Segment Register File Read and Write Pipeline. Rodgers describes "A mechanism and procedure for providing an efficient pipeline for reading and writing information to a multiple ported segment register file (SRF) in different pipe stages." (Abstract). The Examiner references Figure 2A, elements 310-304 and 305 , column 6 lines 49-63 as combining with Bates to arrive at the present disclosure. The Examiner characterizes the execution units 301, 302, 303 and 304 , part of the superscalar execution unit 203 in Rodgers (fig 2A), connected to reservation station as being similar to the the functional units and switches of the present disclosure. Applicant disagrees that one skilled in the art could combine Rodgers and Bates to arrive at the present claims. As amended, the claims require that the interconnected functional units operate independently, while the programmable switches reroute the data flow including tokens to reconfigure the interconnected functional units on command. This teaches away from Rodgers as the structure of the present disclosure is different and functions differently from Rodgers. Rodgers does not suggest nor teach the data flow switching approach of the present disclosure.

The superscalar CPU in Rodgers can execute more than one instruction per clock cycle, however it cannot reconfigure itself, nor respond to reconfiguration com-

mands. A superscalar architecture typically includes parallel, structurally fixed, execution units, which can execute instructions simultaneously. A superscalar architecture of Rodgers does not have switches to direct data streams, including instructions, to interconnected, independently operating functional units.

As stated in Rodgers col 6, line 46 - 54:

Renamed instructions are then passed to reservation station (RS 305) where they remain until their source data becomes valid (e.g. available for use by the execution units). When the source data becomes valid, the instructions of the reservation station 305 may be scheduled for execution and dispatched to an appropriate execution unit within the execution core 203 of the present invention. Multiple instructions may be executed in parallel by the execution core 203 of the present invention.

Thus in Rodgers, only instructions are stored in reservation station 305 to be matched later on to data as it arrives using some other path separate from the instruction path. Specifically, in Rodgers, as detailed in col 6, lines 46-54 instructions are NOT switched along with the data, but only stored until the proper data (to be operated on by the instructions) arrives. This "store, wait and match" approach is structurally different from the present claims where both tokens and data are switched by switches among functional units without requiring storage for waiting data and time delay for instructions to match the data as in Rodgers.

Because the functional units operate independently in the present disclosure, there is no storage location for instructions such reservation station 305 in Rodgers. The switches in the present disclosure are not equivalent to the "store, wait and match" approach in Rodgers as they perform a different function, switching data and tokens, without the storage and delay inherent in Rodgers. There is no suggestion in Rodgers how to convert "store, wait and match" approach to a switch of the present disclosure. A switch of the present disclosure would not work in Rodgers, nor would the "store, wait and match" approach be applicable to the structure of a switch in the present disclosure. Rodgers does not programmably reconfigure a plurality of interconnected functional units to direct a data stream including tokens among a

plurality of interconnected functional units in accordance with software commands. Thus, the present disclosure teaches away from Rodgers.

Pardo et al, U.S.Patent 5,754,839, filed august 28, 1995, describes a single, pipelined processor (110), not a plurality of switch interconnected functional units. Pardo is structurally different from the present application, as it does not reference programmable switches connecting independent functional units. Pardo does not teach nor suggest using the single computer structure in Bates or Rodgers to arrive at a concurrent, multi-processor structure of the present application where tokens are used to change how the data is to be operated on in accordance with said tokens and switches are used to change the configuration of functional units. Pardo does not describe any switching means or other means for re-configuring multiple, independent, concurrently operating functional units.

As amended, the claims of the present application do not read on either Bates, Rodgers or Pardo, or the combination of Bates, Rodgers and Pardo, because the claims as amended describe multiple, independent, concurrently operating functional units responsive to tokens contained within the data stream where the data flow among functional units can be re-configured using switches.

The Examiner has rejected claim 10 over Bates, Rodgers, Pardo,further in view of Master et al. Master at al, U.S. Patent 6,836,839, filed March 22, 2001, does not envision a plurality of functional units, operating concurrently, using a data and tokens as in the amended claims. Master describes " a new category of integrated circuitry and a new methodology for adaptive or reconfigurable computing" (Abstract). The concept of viewpoints generated by a debug stream in conjunction with tokens are not described nor suggested. In fig 3 of Master, a block diagram illustrating a reconfigurable matrix, a plurality of computation units and a plurality of computational elements are shown (Col 4, lines 15-17). In fig 3, there are two distinct busses, Data Interconnect Network 240 and Boolean Interconnect Network 210. As detailed in column 5, starting line 61:

The matrix interconnection network 110 of fig 1, and its subset interconnection

networks separately illustrated in FIGS. 3 and 4 (Boolean interconnection network 210, data interconnection network 240 and interconnect 220..

Continuing on Col 6 , line 15:

In addition, the various interconnection networks (110, 210, 240 and 220) provide selectable or switchable data, input, output, control and configuration paths between and among the controller 120, the memory 140 and various matrices 150, and the computational units 200 and computational elements 250, in lieu of any form of traditional or separate input/output busses, data busses, DMA, RAM configuration or instruction busses.

Thus, Master does not achieve reconfiguration by switching data flows among functional units, but rather by switching separate "data, input, output control and configuration paths". The present disclosure therefore teaches away from Master by switching a data stream containing tokens. The switches in Master would be useless in the present disclosure as their function is different. Master does not suggest the use of its switches in a manner described in the present disclosure, nor would the switches of the present disclosure be applicable in Master.

Thus, the claims as amended, detail the use of tokens in concurrently operating, switch connected re-configurable functional units not present in either Bates, Pardo or Master. The claims are therefore not obvious under 35 USC §103(a) over Bates at al, U.S. Patent 7,080,360 in view of Pardo et al, U.S. Patent 5,754,839, further in view of Master et al, U.S. Patent 6,836,839.

Support for the reference to interconnected switches and functional units and their operation in the amended claims is found in the originally filed specification and the parent application.

Obviousness under 35 USC 103(a)

A time honored test for obviousness upheld by the Supreme Court in *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727 (2007) is summarized by the "suggestion-teaching - motivation" concept. Under this test, a claimed invention cannot be held "obvious" under 35 USC 103 in the absence of some proven "suggestion, teaching or motivation" that would have led a person of ordinary skill in the art to combine prior art teachings in the manner claimed. Setting a threshold for 103 obviousness, and applicable herein, is the holding in *Sakraida v Ag Pro, Inc* 425 US 274, 281-282 (1976) where obviousness was found in a "combination which unites old elements with no change in their respective functions". Unchanged by *KSR*, this test is applicable herein.

The functions of elements in the present invention, as claimed, and explained above, differ substantially from the cited prior art and are not a "combination which unites old elements with no change in their respective functions". Neither Bates, Rodgers, Pardo or Master suggest using tokens within a data stream, where the data stream is steered by a plurality of switch interconnected, reconfigurable, concurrently operating, independent functional units.

In contrast to, and teaching away from the cited prior art, as presently claimed, the present disclosure has a different structure, different elements performing different functions from Bates, Rodgers, Pardo or Master. Thus, the present disclosure is not obvious over Bates, Rodgers Pardo and Master. or a combination of Bates, Rodgers Pardo and Master.

In view of the above, the claims have been amended to reflect the structural differences in the present application over Bates, Rodgers, Pardo and Master thus overcoming the 35 USC 103(a) rejection.

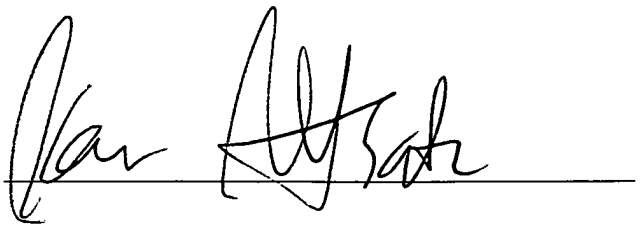
No new matter is introduced by the above.

Having overcome rejections and objections by the Examiner, processing towards

issue of this application is respectfully requested.

FEE CALCULATION - No independent or dependent claims are added. No fee is due.

Respectfully submitted,

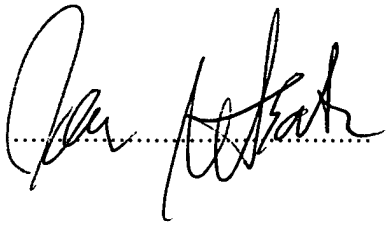


Istrate Ionescu, Attorney for Applicants

Reg. Number 33,185
Tel. No. 203-381-9400
FAX No. 203-381-9401

P.O.Box 697
Stratford, CT. 06614

CERTIFICATE of MAILING:
In accordance with 37 CFR 1.8, I hereby certify that these papers are being mailed by First Class Mail to:
Mail Stop: Amendment
Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Signature: 

DATE: August 18, 2008

Print Name:I.Ionescu